Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1. (Currently amended) A scalable processing system having general purpose registers and a general purpose memory, comprising:

a memory device that is operative to store a plurality of executable program instructions in definable locations, each said executable program instruction being propagated through said memory device, wherein position of each of said executable program instructions in said memory device is associated with a current timetag and each said timetag is indicative of the nominal sequential order of execution of said associated executable program instructions;

a plurality of processing elements distributed throughout said memory device, each of said processing elements being configured and arranged to receive executable program instructions from current positions of said memory device, wherein each of said processing elements executes said executable program instructions associated with said current position without regard to order; and

a plurality of active stations associated with each of said processing elements for enforcing programmatic ordering of said executable program instructions as indicated by the state of said timetag.

2. (Previously presented) The method according to claim 1 wherein said program instructions are propagated in a linear sequence.

3. (Previously presented) The method according to claim 1 wherein said program instructions are propagated in a block.

4. (Previously presented) The method according to claim 1 wherein said program instructions are propagated in columns.

5. (Currently amended) A scalable processing system having general purpose registers and a general purpose memory, comprising:

a memory device that is operative to store a plurality of executable program instructions in definable locations, each said executable program instruction being propagated through said memory device, wherein position of each of said executable program instructions in said memory device is associated with a current timetag and each said timetag is indicative of the nominal sequential order of execution of said associated executable program instructions;

a plurality of processing elements distributed throughout said memory device, each of said processing elements being configured and arranged to receive executable program instructions from current positions of said memory device, wherein each of said processing elements executes said executable program instructions associated with said current positions without regard to order having the highest priority;

a plurality of active stations associated with each of said processing elements for enforcing programmatic ordering of said executable program instructions as indicated by the state of said timetag data field, each of said active stations having a dedicated timetag register for capturing a temporally closest previous broadcast timetag value for comparison with a timetag of a datum sharing a common address in the active station in order to accomplish at least one of the following: a) to enforce said programmatic ordering, b) to link said instruction with a closest previous related instruction as indicated by a common memory address in said general purpose random access memory, a predicate address, or a register address in said general purpose register, ~~and~~ or c) to minimize dependencies among instructions.

6. (Previously presented) A scalable general purpose processing system for assuring correct processing of instructions according to a resource flow execution model, said system comprising:

a plurality of sharing groups;

a plurality of processing elements, each processing element being associated with at least one sharing group, each processing element operative to generate an output result as a result of executing a program instruction;

a plurality of spanning buses of uniform preselected segment length arranged in columns, said spanning buses being of a column height which is independent of bus length;

a forwarding unit associated with each sharing group, each said forwarding unit being operative to store an output result from a processing element, each said forwarding unit in each column being coupled to monitor its corresponding level in an adjacent spanning bus segment;

a memory device coupled to said spanning buses operative to store a plurality of executable program instructions, wherein each of said executable program instructions includes a timetag data field indicative of the nominal sequential order of said associated executable program instructions; and

a plurality of active stations, each of said active stations for holding a single one of said program instructions, said plurality of active stations forming one said sharing group, and each said forwarding unit in a column being coupled to each said sharing group in said column,

each of said processing elements being configured to receive said executable program instructions from said memory device, wherein each of said processing elements is operative to execute any of said executable program instructions as soon as its operand is acquired thereby generating an output result, whereby a plurality of executable program instructions are executed in parallel during each instruction cycle.

7. (Previously presented) The processing system according to claim 6 wherein said spanning buses are arranged in end-to-end fashion.

8. (Previously presented) The processing system according to claim 6 wherein said timetag data field is limited in length in order to permit reuse of values.

9. (Previously presented) The processing system according to claim 7 wherein said spanning bus columns are coupled in a loop.

10. (Previously presented) A scalable processing system, comprising:

a memory device that is operative to store a plurality of executable program instructions in definable locations, each said executable program instruction being propagated through said memory device;

a plurality of processing elements, each of said processing elements associated with an output result that is produced as a result of executing one of said executable program instructions;

a plurality of active stations, each of said active stations for holding a single one of said program instructions, each of said active stations being associated with at least one of said processing elements for execution of said single program instruction; and

a spanning bus structure configured to couple at least some output results associated with said processing elements to at least some of said active stations, each output result having a timetag and an address associated with it,

each of said active stations comprising at least one input, said input having a timetag and an address associated with it, said input being associated with execution of said single program instruction,

each active station further comprising:

first comparison logic operative to compare said timetag associated with its input with said timetag associated with an output result on said spanning bus and to produce a first comparison result;

second comparison logic operative to compare said address associated with its input with an address associated with an output result on said spanning bus and to produce a second comparison result; and

firing logic operative to issue said single program instruction to one of said processing elements multiple times, each time being based on said first comparison result and said second comparison result.

11. (Previously presented) The processing system of claim 10, wherein said spanning bus is further configured to couple outputs of one or more active stations to other active stations.

12. (Previously presented) The processing system of claim 10, wherein said timetags are indicative of a nominal sequential order of execution of said associated executable program instructions.

13. (Previously presented) The processing system of claim 10, wherein said active station further comprises third comparison logic operative to compare a value of said input to a value of an output result on said spanning bus and to produce a third comparison result, said firing logic further operative to issue said program instruction to one of said processing elements multiple times, each time being based on said first comparison result, said second comparison result, and said third comparison result.

14. (Previously presented) The processing system of claim 10 wherein said input is a datum that is used as an operand by said single program instruction.

15. (Previously presented) The processing system of claim 14 wherein said datum is content of a register and said address associated with said process input is information that identifies said register.

16. (Previously presented) The processing system of claim 10 wherein said input is a predicate that is used by a processing element to determine whether said single program instruction is executed.